UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/730,619 | 12/08/2003 | Burkhard Becker | L&L-I0225 | 4277 |

27346 7590 11/26/2008
LERNER GREENBERG STEMER LLP
FOR INFINEON TECHNOLOGIES AG
P.O. BOX 2480
HOLLYWOOD, FL 33022-2480

| EXAMINER | |
|---|---|
| CHOE, YONG J | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2185 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 11/26/2008 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Application Number: 10/730,619
Filing Date: December 08, 2003
Appellant(s): BECKER, BURKHARD

Laurence A. Greenberg
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed 09/08/2008 appealing from the Office action mailed 07/03/2008.

**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board’s decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

No amendment after final has been filed.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant’s statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

| | | |
|---|---|---|
| 4,405,980 | Hess, Bruno M. | 09-1983 |
| 5,150,471 | Tipon et al. | 09-1992 |
| 3,833,888 | stafford et al. | 09-1974 |
| 5,311,523 | Serizawa et al. | 05-1994 |

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 1-3, 5, 6, 11-15, 18 and 20-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hess (US Patent No.: US 4,405,980)** in view of **Tipon et al. (US Patent No.: 5,150,471)**.

**<u>Regarding independent claims 1 and 11</u>,** Hess discloses a method for transmitting data of a plurality of data types between a digital processor and a hardware arithmetic-logic unit, the method which comprises:

associating the hardware arithmetic-logic unit (Fig.1: ALU) with at least one table memory (Fig.1 AKU), the hardware arithmetic-logic unit (Fig.1: ALU) obtaining data required during a computing operation (Fig.1: instruction) from the table memory (Fig.1: AKU) and/or the hardware arithmetic-logic unit storing data computed during a computing operation in the table memory (col.5, lines 54~66); and

Hess further teaches providing the arithmetic computation rule for computing the plurality of addresses in the table memory as an incrementation rule or a decrementation rule (Fig.1: ALU: an arithmetic logic unit (ALU) is a digital circuit that performs arithmetic and logical operations. The ALU is a necessity for a computer because it is guaranteed that a computer will have to compute basic mathematical operations, including addition, subtraction, multiplication, and division. Therefore it is well known to one of ordinary skill in the art that the Arithmetic Logic Unit must provide the arithmetic computation basic rules such as incrementation or decrementation rule in order to compute addresses).

Hess does not specifically teach reading and/or writing from the digital processor to the table memory by:

preselecting a base address in the table memory dependent on a data type of data to be transmitted; computing a plurality of addresses according to a prescribed arithmetic computation rule in hardware by taking the preselected base address as a

starting point resulting in a computed plurality of address; and accessing the table memory with the digital processor using the computed a plurality of addresses for consecutive read access operations and/or consecutive write access operations in the table memory.

However, Tipon et al. teaches reading and/or writing from the digital processor (Fig.1: processor 12) to the table memory by:

preselecting a base address in the table memory (Fig.1: base address register 18) dependent on a data type of data to be transmitted; computing a plurality of addresses according to a prescribed arithmetic computation rule in hardware (Fig.1: ALU 24) by taking the preselected base address as a starting point resulting in a computed plurality of address; and accessing the table memory with the digital processor (Fig.1: processor 12) using the computed a plurality of addresses for consecutive read access operations and/or consecutive write access operations in the table memory (col.3, lines 15~32 and col.6, lines 6~29).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the base address as taught by Tipon et al. into transmitting data of a plurality of data types between a digital processor and a hardware arithmetic-logic unit of Hess in order to increase processing speed (col.2, line 10). Therefore, it would have been obvious to combine the base address as taught by Tipon et al. with transmitting data of a plurality of data types between a digital processor and a hardware arithmetic-logic unit of Hess to obtain the invention.

**Regarding claim 2**, Tipon et al. teaches storing a plurality of base addresses associated with a plurality of different data types in a base address register, the base address that was preselected being one of the plurality of base addresses; and performing the step of preselecting the base address by using the processor to set a selection bit associated with the base address (col.3, lines 20-26 and col.6, lines 6~17).

**Regarding claims 3 and 22**, Tipon et al. teaches prescribing the plurality of base addresses unalterably in hardware (see Fig.1: base address register 18)(col.3, lines 22-26: the base address in the base address register 18 is just an address serving as a reference point("base") for other addresses. Therefore, the base addresses are prescribed unalterably in the base address register.), wherein the plurality of base addresses cannot be processed by the digital processor (col.3, lines 22-26: the base address in the base address register 18 is just an address serving as a reference point("base") for other addresses. Therefore, the base addresses cannot be processed by the digital processor).

**Regarding claim 5**, Tipon et al. teaches programming the base address (Fig.1: base address register) with the digital processor (Fig.1: processor 12).

**Regarding claim 6**, Tipon et al. teaches the digital processor, programming at least one information item selected from a group consisting of information relating to a number of data items being written to or read from a plurality of memory sub areas associated with the base address, information about a block size of data blocks,

information about a decoding rate, and information about utilized convolution polynomials (col.3, lines 49~56).

**Regarding claim 12**, Tipon et al. teaches said base address memory device is an external base address register designed such that in order to select the base address, said processor sets a selection bit associated with the base address (see Fig.1).

**Regarding claim 13**, Hess teaches said base address memory device is a read only memory (col.7, lines 1~5) and Tipon et al. teaches the plurality of base addresses cannot be processed by the digital processor (col.3, lines 22-26: the base address in the base address register 18 is just an address serving as a reference point(“base”) for other addresses. Therefore, the base addresses cannot be processed by the digital processor).

**Regarding claim 14**, Hess et al. teaches wherein said base address memory device is a rewritable memory that can be programmed by the digital processor (col.5, lines 54~57: RAM is a rewritable memory that can be programmed by the digital processor.).

**Regarding claim 15**, Tipon et al. teaches a configuration memory; said table memory including memory sub areas; and said configuration memory for storing information selected from a group consisting of information relating to a number of data items being written to or read from a plurality of said memory sub areas associated with the base address, information about a block size of data blocks, information about

a decoding rate, and information about utilized convolution polynomials (col.3, lines 49~56).

**Regarding claim 18**, Tipon et al. teaches wherein said table memory has a prescribed memory word length (col.5, lines 65~67).

**Regarding claim 20**, Tipon et al. teaches said hardware arithmetic-logic unit includes an equalizer hardware arithmetic-logic unit and a decoder hardware arithmetic-logic unit; said processor includes a data transmission connection to said equalizer hardware arithmetic-logic unit; and said processor includes a data transmission connection to said decoder hardware arithmetic-logic unit (see Fig.1).

**Regarding claims 21 and 23,** Hess further teaches providing the arithmetic computation rule by providing a hardware counter that implements the incrementation rule or a decrementation rule (Fig.1: ALU: It is well known to one of ordinary skill in the art that the Arithmetic Logic Unit must provide the arithmetic computation basic rules such as incrementation or decrementation rule in order to compute addresses).

3. **Claim 7** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Hess (US Patent No.: US 4,405,980)** in view of **Tipon et al. (US Patent No.: 5,150,471)** and in further view of **Stafford et al. (US Patent No.: US 3,833,888)**.

**Regarding claim 7**, Hess and Tipon et al. do not specifically teach providing a first data type of the plurality of data types as soft input values for channel decoding that are intended for a Viterbi decoder hardware arithmetic-logic unit; and with the

digital processor, programming how many soft input values per unit time can be stored in a memory sub area associated with the first data type

However, Stafford et al. teaches providing a first data type of the plurality of data types as soft input values for channel decoding that are intended for a Viterbi decoder hardware arithmetic-logic unit; and with the digital processor, programming how many soft input values per unit time can be stored in a memory sub area associated with the first data type (see abstract) (The Viterbi decoder hardware arithmetic-logic unit is an intended use for channel decoding. Thus, examiner will not give a weight on the Viterbi decoder hardware arithmetic-logic unit for purpose of examination).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the digital processor as taught by Stafford et al. into transmitting data of a plurality of data types between a digital processor and a hardware arithmetic-logic unit of Hess as modified by Tipon et al. in order to provide an enhanced controlling unit in a data processing system (col.2, line 41~42). Therefore, it would have been obvious combine the digital processor as taught by Stafford et al. with transmitting data of a plurality of data types between a digital processor and a hardware arithmetic-logic unit of Hess as modified by Tipon et al. to obtain the invention.

4. **Claims 8 and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hess (US Patent No.: US 4,405,980)** in view of **Tipon et al. (US Patent No.: 5,150,471)** and in further view of **Serizawa et al. (US Patent No.: US 5,311,523)**.

**Regarding claim 19**, Hess and Tipon et al. do not specifically teach said hardware arithmetic-logic unit is a Viterbi hardware arithmetic-logic unit.

However, Serizawa et al. teaches said hardware arithmetic-logic unit is a Viterbi hardware arithmetic-logic unit (Fig.5 is a block diagram showing the structure of the Viterbi algorithm arithmetic).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Viterbi hardware arithmetic-logic unit as taught by Serizawa et al. into transmitting data of a plurality of data types between a digital processor and a hardware arithmetic-logic unit of Hess as modified by Tipon et al. in order to obtain good error rate performance (col.3, line 3).

Therefore, it would have been obvious to combine Viterbi hardware arithmetic-logic unit as taught by Serizawa et al. with transmitting data of a plurality of data types between a digital processor and a hardware arithmetic-logic unit of Hess as modified by Tipon et al. to obtain the invention.

**Regarding claim 8**, Tipon et al. teaches providing a second data type as trace back values computed by a decoder hardware arithmetic-logic unit; and with the digital processor, programming how many states the trace back values need to include (see Fig.1).

Serizawa et al. further teaches computing data by a Viterbi decoder (Fig.5 is a block diagram showing the structure of the Viterbi algorithm arithmetic).

**(10) Response to Argument**

**<u>1st Point of Argument</u>**

Regarding Applicant's appeal brief on page 7, the applicants argue that Hess does not disclose providing an arithmetic computation rule as an incrementation rule or a decrementation rule.

In response to applicant's argument, an **arithmetic logic unit (ALU)** is a digital circuit that performs arithmetic and logical operations. The ALU is a necessity for a computer because it is guaranteed that a computer will have to compute basic mathematical operations, including addition, subtraction, multiplication, and division.

Therefore, Hess clearly teaches providing an arithmetic computation rule as an incrementation rule or a decrementation rule (Fig.1: ALU: It is well known to one of ordinary skill in the art that the Arithmetic Logic Unit must provide the arithmetic computation basic rules such as incrementation or decrementation rule in order to compute addresses).

**<u>2nd Point of Argument</u>**

Regarding Applicant's appeal brief on pages 7&8, the applicants argue that Tipon does not disclose providing an arithmetic computation rule as an incrementation rule or a decrementation rule.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections

are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In this case, Hess clearly teaches providing an arithmetic computation rule as an incrementation rule or a decrementation rule (Fig.1: ALU: It is well known to one of ordinary skill in the art that the Arithmetic Logic Unit must provide the arithmetic computation basic rules such as incrementation or decrementation rule in order to compute addresses) because an **arithmetic logic unit (ALU)** is a digital circuit that performs arithmetic and logical operations. The ALU is a necessity for a computer because it is guaranteed that a computer will have to compute basic mathematical operations, including addition, subtraction, multiplication, and division.

**3rd Point of Argument**

Regarding Applicant's appeal brief on pages 8&9, the applicants argue that Tipon teaches prescribing the plurality of base addresses unalterably in hardware.

In response to applicant's argument, Tipon clearly teaches prescribing the plurality of base addresses unalterably in hardware (see Fig.1: base address register 18)(col.3, lines 22-26: the base address in the base address register 18 is just an address serving as a reference point("base") for other addresses. Therefore, the base addresses are prescribed unalterably in the base address register and the base address cannot be processed by the digital processor.)

**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Yong Choe/

Examiner, Art Unit 2185

Conferees:

/Vincent F. Boccio/

Primary Examiner, Art Unit 2169

/Sanjiv Shah/

Supervisory Patent Examiner, Art Unit 2185